Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A solid-state imaging apparatus that includes an imaging region and a drive circuit region both formed on one semiconductor substrate, the imaging region including an active-type unit pixel in which a photodiode unit generates signal charge by photoelectric conversion and an amplification unit amplifies the signal charge, the drive circuit region being for driving the photodiode unit and the amplification unit, the imaging region and the drive circuit region including one or more transistors respectively, wherein

all the transistors in the imaging region and the drive circuit region have a same channel polarity.

2. (Original) The solid-state imaging apparatus according to Claim 1, wherein the transistors are of an n-channel MOS type.

3. (Original) The solid-state imaging apparatus according to Claim 1, wherein the drive circuit region includes a dynamic circuit that includes a capacitor for accumulating electric charge and a transistor for performing a switching function.

4. (Original) The solid-state imaging apparatus according to Claim 3, wherein the imaging region includes a plurality of active-type unit pixels, and

the drive circuit region includes a pixel selection circuit for selecting one active-type unit pixel from the plurality of active-type unit pixels and a shift resistor circuit for outputting a selection instruction signal to the pixel selection circuit.

5. (Original) The solid-state imaging apparatus according to Claim 1, wherein

the imaging region includes a transistor for performing a switching function based on a signal received from the drive circuit region, and

the signal charge is output to the amplification unit while the transistor for performing the switching function is ON.

6. (Original) The solid-state imaging apparatus according to Claim 1, wherein

the transistor is of a MOS type, of which a gate length is equal to or less than 0.6 μm.

7. (Original) The solid-state imaging apparatus according to Claim 1, wherein

the transistor is of a MOS type, of which a film thickness of a gate insulator is in a range from 1 nm to 20 nm.

8. (Original) The solid-state imaging apparatus according to Claim 1, wherein

the transistor is of a MOS type, and

an insulator that has a film thickness in a range from 1 nm to 20 nm and functions as a capacitor is formed between a gate electrode of the transistor and the semiconductor substrate.

9. (Original) A camera that includes the solid-state imaging apparatus according to Claim 1.

10. (Currently Amended) A manufacturing method for a solid-state imaging apparatus, comprising steps of:

forming, on a semiconductor substrate, an imaging region including a photodiode unit for converting input light into signal charge and an amplification unit for amplifying the signal charge; and

forming, on the semiconductor substrate, a drive circuit region for driving the imaging region, wherein

~~MOS type transistors having a same channel polarity are~~ all transistors formed in both steps for forming the imaging region and the drive circuit region respectively are MOS type transistors having a same channel polarity.

11. (Original) The manufacturing method for a solid-state imaging apparatus according to Claim 10, wherein

the MOS type transistors formed in the both steps are of n-channel MOS type.

12. (Original) The manufacturing method for a solid-state imaging apparatus according to Claim 10, wherein

a gate length of each MOS type transistor is equal to or less than 0.6 μm.

13. (Original) The manufacturing method for a solid-state imaging apparatus according to Claim 10, wherein

a film thickness of a gate insulator in each MOS type transistor is in a range from 1 nm to 20 nm.

14. (Original) The manufacturing method for a solid-state imaging apparatus according to Claim 10, wherein

an insulator that has a film thickness in a range from 1 nm to 20 nm and functions as a capacitor is formed between a gate electrode of each MOS type transistor and the semiconductor substrate.